this is claim 11.

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11. (Previously presented) The method according to claim 8, wherein said selection step comprises a demultiplexing step of demultiplexing said result and said register address to said selected register files in response to said corresponding indication.

REMARKS

Entry of this amendment and reconsideration are respectfully requested in view of the amendments made to the claims and for the remarks made herein.

Claims 1-11 are pending and stand rejected.

Claims 1-11 stand rejected under 35 USC 103(a) as being unpatentable over Tremblay (WO 00/33178) in view of Hirosawa (USP no 4,975,836) in view of Dictionary of IEEE, 2000, 7th Edition, page 494. The Office Action states the "[i]t would have been obvious to one of ordinary skill ... to use Hirosawa in Tremblay for including the selection of register files as claimed because the use of Hirosawa could provide Tremblay the ability to designate a predefined set of registers based on a given system conditions and therefore, increasing the adaptability of the storage access control in Tremblay and it could be done by configuring the selection circuit of Hirosawa into Tremblay with modified control parameter so that the specific selection of the register files of Hirosawa could be recognized by Tremblay and because Tremblay also taught that his local register were addressed in a local register range outside the global register range (see abstract), which was an indication of the need of the selection of a specific register group to accept address range outside the global range in order to provide enhanced flexibility of the storage control, and in doing so, provided a motivation." (Office Action, item 7, pp. 5-6).

Applicant respectfully disagrees with, and explicitly traverses, the reason for rejecting the claims.

Tremblay, discloses a VLIW processor including a plurality of functional units which include a plurality of separate register file segments, each being associated with one of the functional units. The register file segments are partitioned into local registers and global registers, wherein the global registers are written/read by all the functional units and the local registers are written/read only by the associated functional unit. Tremblay describes, with reference to Figure 6, that the global registers are addressed